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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,038	YEH, TSE-YU	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/10/02; 11/20/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been considered.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 10, element 116. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claim 27 is objected to because of the following informalities: Please correct "A more carrier medium" to read --A carrier medium--. Appropriate correction is required.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claim 27 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claim recites "A more (sic) carrier medium comprising one or more data structures representing a processor", however, this is not the same as a computer readable medium and an entire program cannot be represented on a carrier medium, i.e. single computer signal.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-27 are rejected under 35 U.S.C. 102(b) as being taught by Sager, U.S. Patent Number 5,966,544 (herein referred to as Sager).

10. Referring to claim 1, Sager has taught a processor comprising:

a. A queue configured to store one or more instructions (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8); and

b. A control circuit coupled to the queue, wherein the control circuit is configured to detect a replay of a first instruction due to a dependency on a load miss, and wherein the control circuit is configured to inhibit issuance of the one or more instructions in the queue to one or more pipelines of the processor responsive to detecting the replay (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

11. Referring to claim 2, Sager has taught wherein the control circuit is configured to inhibit issuance of the one or more instructions until fill data is provided to a data cache of the processor (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

12. Referring to claim 6, Sager has taught wherein the control circuit is configured to permit issuance of the one or more instructions in response to fill data being provided to a data cache of the processor (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

13. Referring to claims 3 and 7, Sager has taught wherein the fill data corresponds to the load miss (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

14. Referring to claims 4 and 8, Sager has taught wherein the control circuit includes a storage device, and wherein the control circuit is configured to read a miss tag from a read queue that stores one or more load misses, the miss tag identifying the load miss on which the first instruction is dependent, and wherein the control circuit is configured to store the miss tag in the storage device, and wherein the control circuit further includes a comparator coupled to the storage device and coupled to receive a fill tag identifying fill data being provided to the data cache, and wherein the comparator is configured to compare the miss tag stored therein to the fill tag to determine if the fill data corresponds to the load miss (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

15. Referring to claims 5 and 9, Sager has taught wherein the fill data corresponds to any load miss (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

16. Referring to claim 10, Sager has taught wherein the control circuit is configured to permit issuance of one of the one or more instructions if one or more issue criteria are fulfilled for that instruction (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

17. Referring to claim 11, Sager has taught wherein the one or more issue criteria includes a lack of dependencies being detected for that instruction in one or more scoreboards coupled to the control circuit (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62;

column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

18. Referring to claim 12, Sager has taught wherein the control circuit is configured to detect the dependency of the first instruction on the load miss using one or more scoreboards which track instructions that have passed a first stage of the one or more pipelines, wherein the first stage *is* the stage at which replay is signaled (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

19. Referring to claim 13, Sager has taught wherein the one or more instructions in the queue include the first instruction (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

20. Referring to claim 14, Sager has taught a method comprising:

a. Detecting a replay of a first instruction due to a dependency on a load miss (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8); and

b. Inhibiting issuance of one or more instructions from a queue to one or more pipelines of the processor responsive to detecting the replay (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

21. Referring to claim 15, Sager has taught inhibiting issuance of the one or more instructions until fill data is provided to a data cache (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

22. Referring to claim 19, Sager has taught permitting issuance of the one or more instructions in response to fill data being provided to a data cache of the processor (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

23. Referring to claims 16 and 20, Sager has taught wherein the fill data corresponds to the load miss (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

24. Referring to claims 17 and 21, Sager has taught

a. Reading a miss tag from a read queue that stores one or more load misses, wherein the miss tag identifies the load miss on which the first instruction is dependent (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8); and

b. Comparing the miss tag to a fill tag identifying the fill data to determine if the fill data corresponds to the load miss (Sager Abstract; column 8, lines 15-28 and 54-

63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

25. Referring to claims 18 and 22, Sager has taught wherein the fill data corresponds to any load miss (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

26. Referring to claim 23, Sager has taught wherein the permitting issuance of one of the one or more instructions is responsive to one or more issue criteria being fulfilled for that instruction (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

27. Referring to claim 24, Sager has taught wherein the one or more issue criteria includes detecting a lack of dependencies for that instruction in one or more scoreboards (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

28. Referring to claim 25, Sager has taught wherein the detecting the dependency comprises checking one or more scoreboards which track instructions that have passed a first stage of the one or more pipelines, wherein the first stage is the stage at which replay is signaled (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

29. Referring to claim 26, Sager has taught wherein the one or more instructions in the queue include the first instruction (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

30. Referring to claim 27, Sager has taught a carrier medium comprising one or more data structures representing a processor including:

a. A queue configured to store one or more instructions (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8); and

b. A control circuit coupled to the queue, wherein the control circuit is configured to detect a replay of a first instruction due to a dependency on a load miss, and wherein the control circuit is configured to inhibit issuance of the one or more instructions in the queue to one or more pipelines of the processor responsive to detecting the replay (Sager Abstract; column 8, lines 15-28 and 54-63; column 9, lines 31-62; column 10, lines 8-46; column 11, line 13 to column 12, line 26; column 12, line 47 to column 13, line 32; Figure 7; and Figure 8).

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by

the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Amerson et al., U.S. Patent Number 5,475,823, has taught a memory processor which reissues instructions when an instruction has been incorrectly executed.

b. Brown, III et al., U.S. Patent Number 5,488,730, has taught a scoreboard for a pipelined processor to determine instruction conflicts and dependencies.

c. Leibholz et al., U.S. Patent Number 6,098,166, has taught reissuing instructions on a cache miss.

d. Merchant et al., U.S. Patent Numbers 6,163,838; 6,212,626; 6,385,715; and 6,665,792, have taught a replay system.

e. Tiwari et al., U.S. Patent Number 6,609,209, has taught a replay system which also reduces power consummation.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
September 22, 2004

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